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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. |
|---|---|---|---|
| 09/256,265 | 02/23/99 | KAO | D 16405-311 |

025696 MMC1/0718
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| EXAMINER | |
|---|---|
| DIAZ,J | |
| **ART UNIT** | **PAPER NUMBER** |
| 2815 | |

**DATE MAILED:** 07/18/01

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/256,265 | KAO ET AL. | |
| | Examiner | Art Unit | |
| | José R. Díaz | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *03 May 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,2,8-10,16 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 8-10, 16-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

➢ The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 16 and 17 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 16 and 17 recites the new limitations "a drain region formed...proximate said erase gate; and a source region formed...proximate said control gate", which are not supported by the specification. For example figures 1-2, 3d, and 5d show that the drain region is formed proximate to the control gate and the source is formed proximate to the erase gate. Applicant is required to cancel the new matter in the reply to this Office Action.

### *Claim Rejections - 35 USC § 102*

➢ The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

➢ Claims 1 and 16 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Middelhoek et al. (US Patent No. 5,216,269).

Regarding claims 1 and 16, Middelhoek et al. teach a substrate; a defined channel region; a floating gate (11) disposed over said channel region separated therefrom by a first insulating layer (21); a control gate (12) placed on one side of said floating gate (11) separated therefrom by a second insulating layer (22); a erase gate (14) placed on second side of said floating gate (11) separated therefrom by said second insulating layer (22); a drain region (6) disposed on a first side of said floating gate (11); and a source region (5) disposed on a second side of said floating gate (11) (Figure 10).

➢ Claims 8 and 10 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Chang (US Patent No. 6,125,060).

Regarding claim 8, Chang teaches a memory array (214) comprising a plurality of memory cells each having a floating gate (103), an erase gate (122), a control gate (101), a source region (105), and a drain region (108) (Figure 1f) comprising: a plurality of rows and columns of interconnected memory cells wherein the control gates (CG(i)) of memory cells in the same row are connected by a common word-line (201); the erase gates (EG(m)) of memory cells in the same row are connected by a common erase-line (207); the source regions (Source(m)) of memory cells in the same row are connected by a common source-line (205); the drain regions (208) of memory cells in the same row are connected by a common drain-line (BL (i)); and control circuit connecting to

circuit connecting to said word-lines, erase lines, source lines and drain lines for operating one or more memory cells of said memory array (Figure 3).

Regarding claim 10, Chang teaches that said erase gate (122) overlaps said floating gate (103) and said control gate (101) (Figure 1f).

***Claim Rejections - 35 USC § 103***

➢ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

➢ This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

➢ Claims 2 and 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Middelhoek et al. (US Patent No. 5,216,269) in view of Chang (US Patent No. 6,125,060).

Regarding claims 2 and 17, Middelhoek et al., as stated supra, essentially discloses the claimed invention but fails to show a transistor wherein an erase gate overlaps a floating gate and a control gate. Chang teaches that said erase gate (122) overlaps said floating gate (103) and said control gate (101) (Figure 1f). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Middelhoek et al. to include the limitation wherein said erase gate overlaps said floating gate and said control gate. The ordinary artisan would have been motivated to modify Middelhoek et al. in the manner described above for at least the purpose of manufacturing a memory device having low currents for both program and erase operations.

- Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (US Patent No. 6,125,060) in view of Middelhoek et al. (US Patent No. 5,216,269).

Regarding claim 9, Chang, as stated supra, essentially discloses the claimed invention but fails to show an erase gate placed on a second side of a floating gate separated therefrom by a second insulation layer. Middelhoek et al. teach a substrate; a defined channel region; a floating gate (11) disposed over said channel region separated therefrom by a first insulating layer (21); a control gate (12) placed on one side of said floating gate (11) separated therefrom by a second insulating layer (22); a erase gate (14) placed on second side of said floating gate (11) separated therefrom by said second insulating layer (22); a drain region (6) disposed on a first side of said floating gate (11); and a source region (5) disposed on a second side of said floating gate (11) (Figure 10). Therefore, it would have been obvious to one having ordinary skill

in the art at the same time the invention was made to modify Chang to include an erase gate placed on a second side of a floating gate separated therefrom by a second insulation layer. The ordinary artisan would have been motivated to modify Middelhoek et al. in the manner described above for at least the purpose of forming a feed-back loop to prevent over-erasure.

***Response to Arguments***

➢ Applicant's arguments filed February 6, 2001 have been fully considered but they are not persuasive. Applicant argues that the prior art does not disclose "a semiconductor device wherein at least a portion of said control gate is disposed over a portion of said substrate and is separated therefrom by said second insulating layer." Examiner disagrees because the prior art Middelhoek et al. does teach the limitation in Figure 10. Middelhoek et al. show in Figure 10 that the control gate (12) is formed over a top portion of the floating gate (11) separated by an insulating layer (e.g. the layer between the control gate 12 and the floating gate 11); over or above one of the sidewall of the floating gate (e.g. the sidewall of the floating gate proximate to the drain region 6), over portion of the channel (e.g. region between the source 5 and the drain 6), and over portion of the substrate (e.g. region which comprises the drain region 6 and region 3). Therefore, the prior art Middelhoek et al. anticipates the claimed limitation.

➢ Applicant's arguments with respect to claims 16-17 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

➢ Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

***Correspondence***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 8:00 - 5:00 Monday through Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD
July 11, 2001

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800